REMARKS/ARGUMENTS

In response to the Office Action dated November 29, 2002, claim 18 is amended and claims 19-20 are canceled without prejudice or waiver. Claims 1-17 were previously canceled without prejudice or waiver. Claim 18 and 21 remain in the application. Figure 10(a) is also corrected, and a substitute sheet is attached. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Correction to the Drawings

Figure 10(a) is corrected herein and a substitute sheet is attached. The changes presented herein are supported by the specification on Page 9, lines 19-23 and page 9, line 36 through page 10, line 2. No new matter has been added.

Non-Art-Based Rejections

On page 2 of the Office Action, claims 18-21 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention.

Specifically, the Office Action recited as grounds for the rejection the second silicon nitride layer on the source/drain diffusion layers set forth in the claims as not being supported in the specification.

The Applicants respectfully traverse the rejection, and direct the Examiner to the specification at Page 7, lines 11-15, where the second silicon nitride layer on the source/drain diffusion layers is discussed:

> On opposite side walls of the gates in each memory cell, first silicon nitride film 10 are formed by low-pressure CVD. Then a second silicon nitride film 11 is formed to cover surfaces of the control gate 6, silicon nitride films 10 on the side walls, source and drain diffusion layers 7a and 7b.

The Applicants respectfully submit that the claims are supported by the specification, and that the rejection should be withdrawn.

On pages 2-3 of the Office Action, claims 18-21 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

Specifically, the Office Action recited as grounds for rejection plural recitations of the limitation "layer" in the claims.

Applicant respectfully traverses the rejections, but, in order to expedite prosecution of the application, has amended the claims. Each recitation of "layer" in the claims contains additional identifying language, e.g., "source/drain diffusion layers," to clarify which layer is being referred to. Applicant believes that any amendments made under this section merely clarify the claim language, and do not surrender any equivalents because of such amendments. It is not Applicant's intent to surrender any equivalents due to amendments made which may touch upon these rejections.

Art-Based Rejections

On pages 3-6 of the Office Action, claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Mehrad et al., USPN 6,071,779, in view of Mori (JP407161848). Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mehrad et al., in view of Mori and further in view of Sato (USPN 5,962,890). Claim 21 was rejected under 35 U.S.C. § 103(a) as being unpatentable

over Mehrad et al., in view of Mori and further in view of Santin et al. (USPN 5,907,171).

The Applicants respectfully traverse the rejections in light of the amendments above and the arguments set forth below. The Applicants respectfully submit that the claims are patentable in light of the clarifying amendments above and the arguments below.

The Mehrad Reference

The Mehrad reference discloses a method of fabricating a semiconductor device having a memory array. Sourse line 24 connects the sources 12 to each other by a continuous conductive region formed within the semiconductor substrate 52 proximate ths source region 60. As best illustrated in FIG. 3, the source line 24 crosses the isolation structures 70 in the source region 60 of the semiconductor substrate 52 below the isolation structures 70. In contrast, the isolation structures 70 electrically isolate the adjacent floating gate transistors 11 in the channel region 64 of the semiconductor substrate. See Col. 6, line 65-Col. 7, line 7.

The Mori Reference

The Mori reference discloses a two layered gate present on a silicon substrate. The two layers of gate are a control gate electrode and a floating gate. A first silicon nitride film is present on the side walls of the two gate electrodes. A second silicon nitride film is provided on the side wall of silicon oxide film. See Abstract translation.

The Sato Reference

The Sato reference discloses a semiconductor memory in which a plurality of flash memory cells are arranged in a matrix, each flash memory cell including source and drain regions formed on a silicon substrate. A common source line for connecting the source region of the flash memory cells includes a diffusion layer formed in the silicon substrate and a silicide layer formed on the diffusion layer. See Abstract.

The Santin Reference

The Santin reference discloses a memory encased in a P-well, and the P-well encased in a deep N-well, the two wells separating the memory array from the integrated circuit substrate and from the other circuitry of the integrated circuit. See Abstract.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe A nonvolatile semiconductor memory device comprising a semiconductor substrate, shallow trench isolation layers, memory transistors, and sidewalls and layers formed of silicon nitride.

The shallow trench isolation layers are strip shaped and extend in one direction. They are embedded in a surface of the semiconductor substrate with predetermined intervals. A strip-shaped memory region is formed between two adjacent shallow trench isolation layers, and two adjacent memory regions are isolated by one of said shallow trench isolation layers.

The memory transistors are formed in each of said memory regions and perform nonvolatile storage of data. Each memory transistor comprises a floating gate which is formed on said semiconductor substrate via a first gate insulating layer, a strip-shaped control gate which is formed on said floating gate via a second gate insulating layer, said control gate extending in another direction perpendicular to said one direction, and said control gate being common to said memory transistors,

and two source/drain diffusion layers formed on the surface of said semiconductor substrate.

The sidewalls are formed of a first silicon nitride layer, and cover both sides of said floating gate and said control gate of each of said memory transistors. The sidewalls are formed via an oxide layer serving as a stopper at the time of the etching for forming said sidewalls.

Layers are formed of a second silicon nitride layer, each covering at least the upper surfaces of the control gate and surfaces of the sidewalls of each of the transistors. Each layer is removed by etching so as not to exist on said source/drain diffusion layers so that the source/drain diffusion layers are exposed. The nonvolatile semiconductor memory device further comprises silicide layers formed on the surfaces of said control gate and said source/drain diffusion layers in each of said memory transistors, wherein in each of said memory transistors, one of the two source/drain diffusion layers is connected to a bit line via said silicide layer, and the other is connected to a common source line via said silicide layer, wherein said nonvolatile semiconductor memory device further comprises strip-shaped common source lines extending in said another direction, said each common source line being embedded in an interlayer insulation film between adjacent two of said control gates, the bottom surface of each said common source line being connected to said silicide layers which are formed on the surface of said others of said two source/drain diffusion layers and which are arranged in said another direction.

The cited references do not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited references does not teach nor suggest the limitation of each common source line being embedded in an interlayer insulation film as recited in the claims of the present invention.

The cited references show that the source lines (source/drain diffusion layers) are formed within the substrate, not within an interlayer insulation film. See Mehrad, Col. 6, line 65-Col. 7, line 7. Similarly, Sato teaches that the source lines are formed within the substrate. See Sato, Abstract, lines 11-14. Santin teaches that the

memory cell is buried in a p-well which is buried in an n-well. See Santin, Abstract. Mori does not teach an interlayer insulation film.

As such, there is no teaching of the limitation of each common source line being embedded in an interlayer insulation film as recited in the claims of the present invention.

The advantage of embedding the common source lines into the interlayer insulation film rather than in the substrate is that it is easier to thicken the common source lines. Further, the silicide layers on the source diffusion layers in line are electrically connected to one common source line corresponding thereto, and thereby the source diffusion layers in line are connected to each other. As a result, it is possible to connect the source diffusion layers with lower resistance.

In addition, in forming the common source lines, the source diffusion layers in line are automatically connected serially via the silicide layer on the source diffusion layers with lower electric resistance. None of these advantages are taught nor suggested by any of the cited references, alone or in combination.

Thus, it is submitted that independent claim 18 is patentable over the cited references. Claim 21 is also patentable over the cited references, not only because claim 21 contains all of the limitations of the independent claim 18, but because claim 21 also describes additional novel elements and features that are not described in the prior art.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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